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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/787,094	02/27/2004	Eric Boisvert	101783-6	4814

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EXAMINER	
HAILU, KIBROM T	

ART UNIT	PAPER NUMBER
2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/787,094	BOISVERT ET AL.	
	Examiner	Art Unit	
	Kibrom T. Hailu	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 3, 9, 10, 11, 12, 16 and 20 are objected to because of the following informalities:

Regarding claims 3, 9, 12, 16 and 20, the limitation abbreviations "DMA" and "CSUM" used for Direct Memory Access and Checksum, respectively should be defined in the claims at least where it is first used. Appropriate correction is required.

Regarding claims 10 and 11, a "comparitor" is assumed to be "comparator". Correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-7, 9 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Boucher et al. (US 6,434,620 B1).

Regarding claim 1, Boucher discloses an apparatus providing a specialized microprocessor or hardwired circuitry (Abstract, "intelligent network interface card, INIC") to process packets for data communications and control (col. 5, lines 31-45) comprising: a) a microprocessor (pipelined microprocessor 470) in communication with a memory (Fig. 21, SRAM) for data and program storage (Figs 21 and 22), the processor (470) configured to process instruction words of a fixed length of bits (col. 76, lines 51-59) and to decode (instruction decoder and operand multiplexer 498) not more than four instructions (Fig. 22; col. 80, lines 5-

24); b) two general-purpose registers in communication with the microprocessor (col. 63, lines 21-23, 37-42, "general event register" and "the channel event register", which are comprised in the INIC and in communication with the processor 470); and c) a state machine (Figs 19 and 20, "state diagram") controlling the operation of the microprocessor (Figs 19 and 20; col. 61, lines 63-65), the state machine having four states, a RESET state (col. 50, lines 31-33), a FETCH state (col. 79, lines 11-19, 62-65; col. 80, line 63-col. 81, line 1), a WAIT state (col. 40, lines 49-52; col. 73, lines 6-10) and a JUMP state (col. 74, lines 18-33; col. 81, lines 57-59; col. 82, line 34-col. 83, line 5).

Regarding claim 2, Boucher further discloses including: a) means to handle internal events coupled to said microprocessor (col. 63, lines 17-43; col. 40, lines 52-53) and b) means to handle external events coupled to said microprocessor (col. 63, lines 48-55);

Regarding claim 3, Boucher further discloses including a DMA register coupled to said microprocessor (see Fig. 21).

Regarding claim 4, Boucher discloses including at least one timer coupled to said microprocessor (col. 40, lines 52-53; col. 63, lines 21-23; col. 67, lines 25-26).

Regarding claim 5, Boucher discloses the packets are Internet protocol packets (col. 5, lines 48-56).

Regarding claim 6, Boucher discloses the means to handle internal events is responsive to events originating from at least one of: a) timers; b) real-time timers; or c) watchdog logic (col. 40, lines 52-53; col. 63, lines 21-23; col. 67, lines 25-26; col. 74, lines 27-28. Note also that watchdog logic is known in the art, see Chapman et al. (US 6,594,774), col. 2, lines 25-32).

Regarding claim 7, Boucher discloses the means to handle external events is responsive to events originating from: a) the reception of a packet (col. 89, lines 19-23, 43-45); b) notification that data is ready to be transmitted (col. 89, lines 48-57); or c) notification that data has been transmitted (col. 89, lines 62-65).

Regarding claim 9, Boucher further discloses including a CSUM register and a DMA register coupled to said microprocessor (Fig. 21; col. 7, lines 61-63; col. 11, lines 57-60;...when a frame is received by the INIC, the checksum is calculated and verified in the INIC. Therefore, it would be obvious the presence of checksum register).

Regarding claim 20, the claimed limitations include the features corresponding to the subject matter mentioned above in the rejected claims 1, 2, 4 and 9, and the same rejections applied hereto.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Boucher in view of Westermeier (US 2003/0048775 A1).

Regarding claim 8, Boucher doesn't explicitly disclose the packets contain video information.

Westermeier teaches the packets contain actual user information such as video or voice data (paragraph [0014]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the data packets of Westermeier that contain video information into data communication of Boucher so that time sensitive information can reliably be delivered.

7. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boucher in view of Dupree at al. (US 5,655,133).

Regarding claims 10 and 11, Boucher discloses registers comprised in the INIC or the data communication-processing device. However Boucher doesn't disclose a comparator coupled to both said general-purpose registers to produce an output to the microprocessor representative of the relative data content between the two registers, and the comparator output is a pair of flags, namely, an equal flag and a greater than flag.

Dupree teaches a comparator (comparator circuit 108) coupled to both said general-purpose registers (general purpose registers 100) (Fig. 2; col. 6, lines 18-22) to produce an output to the microprocessor representative of the relative data content between the two registers (col. 7, lines 39-43), and the comparator output is a pair of flags, namely, an equal flag and a greater than flag (col. 7, lines 48-53).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to use the comparator circuit 108 coupled to the general-purpose registers 100 and outputs the comparison operations result as taught Dupree into the data communication processing device of Boucher to achieve a fast and a substantial degree of design and programming flexibility.

8. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Boucher in view of Beverly (US 7,020,836 B2).

Regarding claim 12, Boucher discloses a CSUM register coupled to the microprocessor over a data path, the CSUM register configured to calculate the checksum of each instruction word received over the data path (col. 5, lines 50-53; col. 62, lines 65-67; col. 67, lines 66-67; col. 68, lines 32-37). However, Boucher doesn't explicitly disclose the checksum calculation is based a one's complement.

Beverly teaches calculating a one's complement checksum (col. 2, lines 16-30; claim 1 and 13).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to compute the one's complement checksum as taught by Beverly and use it into the data communication processing device of Boucher so that the requirement of significant mathematical, power consumption and integrated circuit die space would be reduced (Beverly, col. 1, lines 45-52).

9. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Boucher in view of Beverly, as applied to claim 12 above, and further in view of Boyle et al. (US 6,092,229).

Regarding claim 13, Boucher discloses calculates a checksum value (col. 5, lines 50-53; col. 62, lines 65-67; col. 67, lines 66-67; col. 68, lines 32-37). However, Boucher doesn't explicitly disclose the calculated checksum value is equal to or matches a pre-chosen value.

Boyle teaches the calculated checksum value matches or equal to the predetermined of a pre-chosen value (abstract; col. 6, line 61-col. 7, line 2; col. 2, lines 9-14, 24-25).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the comparison system of Boyle that matches the calculated checksum with the predetermined or pre-chosen value into the checksum calculation of Boucher in order to provide a valid information to local device memory (Boyle, col. 2, lines 14-15).

10. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Boucher in view of Gates (US 6,449,709 B1) and further in view of Warnes (US 7,051,189 B2).

Regarding claim 14, Boucher discloses instructions (such as halt, run, step, dump, load and break). However, Boucher doesn't explicitly disclose the MOVE instruction has 14 bits dedicated to define a source address and 14 bits dedicated to define a destination address.

Gates discloses MOV instruction for moving data from source address to destination address (col. 5, lines 29-32). However, Gates doesn't teach the MOV instruction is dedicated to move 14 bits.

Warnes teaches 14 bits move/compare instruction to define the source/destination addresses (see claim 35).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the move instruction of Gates dedicated to move data from the source address to the destination address and the 14 bit move instruction of Warnes into the data

communication processing device of Boucher in order to reduce the clock frequency so that the speed of the overall performance of the system would be improved.

11. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boucher in view of Warnes.

Claim 15 is the same as claim 1 except now instructions LOAD and MOVE are explicitly claimed, as noted above, Warnes teaches the two instructions (see claim 35).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the move and load instructions of Warnes into the data communication-processing device of Boucher in order to reduce the clock frequency so that the speed of the overall performance of the system would be improved.

Regarding claim 16, which inherits the limitations of claim 15, the claimed limitations include the features corresponding to the subject matter mentioned above in the rejected claims 2, 4 and 9, and the same rejections applied hereto.

Regarding claim 17, which inherits the limitations of claim 16, the claimed limitations include the features corresponding to the subject matter mentioned above in the rejected claim 5, and the same rejections applied hereto.

12. Claims 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boucher in view of Warnes, as applied to claim 17 above, and further in view of Westermeier.

Regarding claim 18, which inherits the limitations of claim 17, the claimed limitations include the features corresponding to the subject matter mentioned above in the rejected claim 8, and the same rejections applied hereto.

Regarding claim 19, which inherits the limitations of claim 18, the claimed limitations include the features corresponding to the subject matter mentioned above in the rejected claim 7, and the same rejections applied hereto.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kibrom T. Hailu whose telephone number is (571)270-1209. The examiner can normally be reached on Monday-Thursday 8:30AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Q. Ngo can be reached on (571)272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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07/05/2007

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